Benefits and Issues on Migration of 5-V and 3.3-V Logic to Lower-Voltage Supplies

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Contents

List of Illustrations

List of Tables

Abstract

In the last few years, the trend toward reducing supply voltage (V_{CC}) has continued, as reflected in an additional specification of 2.5-V V_{CC} for the AVC, ALVT, ALVC, LVC, LV, and the CBTLV families.

In this application report, the different logic levels at V_{CC} of 5 V, 3.3 V, 2.5 V, and 1.8 V are compared. Within the report, the possibilities for migration from 5-V logic and 3.3-V logic families to 2.5-V V_{CC} are shown, and the implications of the reduced supply voltage are discussed. Data is provided that shows the influence of reduced V_{CC} on power consumption, drive capability, and propagation delay time for the logic families.

Further, the requirements for an overvoltage tolerance (5-V/3.3-V input and output) is discussed, as well as interfacing opportunities in a mixed-mode environment in which two different supply voltages are used.

This application report is intended to be used as a designer's guide to component selection and usage at supply voltages below 3.3-V. The data in this document is typical data taken under typical laboratory conditions (25°C) and 2.5-V or 1.8-V, except where otherwise noted. The data is intended as a design guideline only.

Background

The use of 5-V V_{CC} has long been the standard for both core and memory logic. However, with the increase in complexity and the functionality of application-specific integrated circuits (ASICs), central processing units (CPUs), microprocessors, and digital signal processors (DSPs), it has become necessary to reduce the structure size of these elements.

Using modern manufacturing processes that produce smaller structures, the thickness of the gate oxide of each single transistor has become more sensitive to electrostatic field strength. Because the field strength is proportional to the supply voltage, the direct result is that supply voltage must be reduced for a reliable operation.

In other words, making electronic devices more complex, without enlarging the overall size of the chip area, requires reducing the structure size, which also requires reducing V_{CC}.

The limit for reliable operation at less than 5-V V_{CC} is reached at a structure size of 0.6 micron, and the use of a 0.35-micron manufacturing process requires 2.5-V V_{CC} for proper operation.

Moreover, power consumption always is a concern for new system designs. A reduction in supply voltage produces an exponential decrease in power consumption; therefore, the trend is to reduce power-supply voltage. To meet these requirements, many modern logic families are specified at different voltage nodes, which enables designers to use them at 3.3-V V_{CC} and at 2.5-V V_{CC}.

This application report investigates the possibilities for migration of 5-V and 3.3-V logic to 2.5-V logic, and discusses the implications.

Input- and Output-Level Specifications at Different Supply Voltages

For each V_{CC} a standard is defined, with commonly agreed-upon levels of input and output levels. Figure 1 shows the appropriate switching levels for 5-V, 3.3-V, and 2.5-V that have passed the JEDEC committee. Additionally, the 1.8-V level specification, as given in the data sheets of the SN74LVCxxxA and SN74AVCxxx devices, is shown.

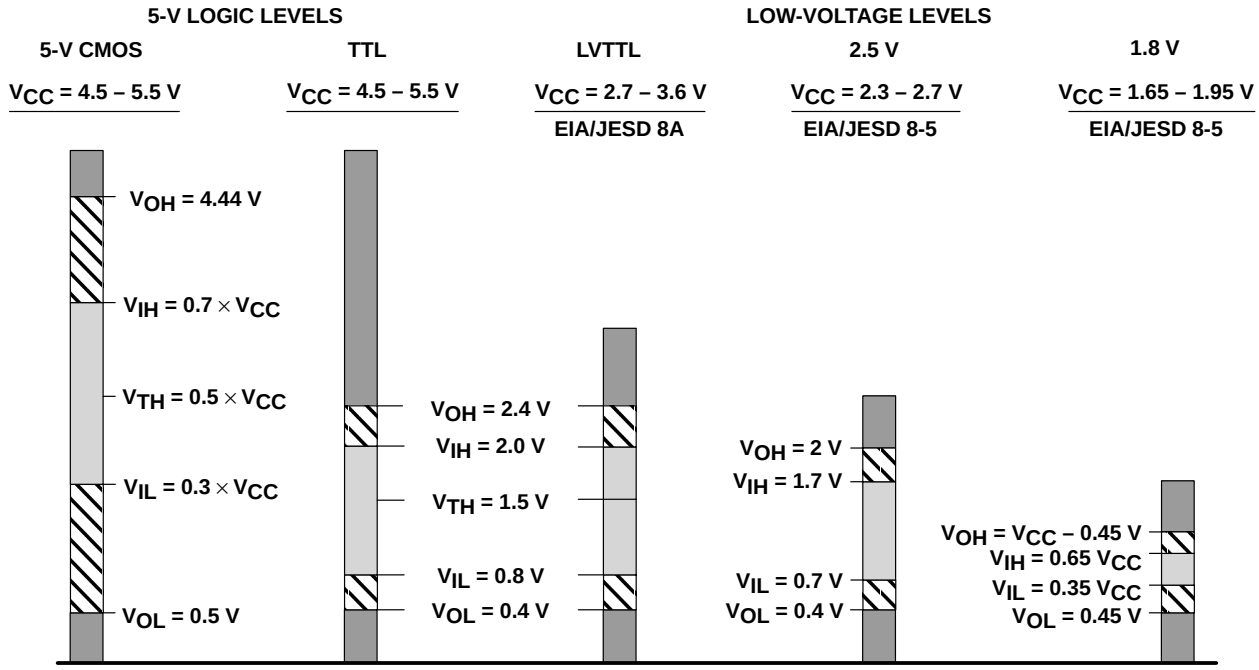


Figure 1. 5-V, 3.3-V, and 2.5-V Switching-Level Comparison

Table 1 contains additional information regarding the various logic families, including manufacturing process, the optimal power supply, and the V_{CC} at which the logic families are functional.

The AHC family is included in this overview. Although the AHC family was targeted for the 5-V V_{CC}, after its market introduction, this family also was specified for operation at 3.3 V V_{CC}.

The low-voltage logic families (SN74LVxxxA, SN74LVCxxxA, SN7ALVCHxxx) also have been characterized at 2.5-V V_{CC}, to meet the trend of reduced supply voltages.

The AVC family is the optimal solution for 2.5-V V_{CC}, and also is fully characterized at 1.8-V and 3.3-V V_{CC}.

The data sheets for the LVC family show switching characteristics at 1.8-V V_{CC}.

Table 1. Operational Supply Voltages of Different Logic Families

LOGIC FAMILY	MANUFACTURING PROCESS	OPTIMAL POWER-SUPPLY LEVEL	OPERATIONAL AT V_{CC} = 3.3 V	OPERATIONAL AT V_{CC} = 2.5 V	OPERATIONAL AT V_{CC} = 1.8 V
AHC	CMOS	5 V	Fully specified	Yes, down to 2 V	Not specified
ALVC	CMOS	3.3 V	Fully specified	Fully specified	Planned
ALVT	BiCMOS	3.3 V	Fully specified	Fully specified	Not specified
AVC	CMOS	2.5 V	Fully specified	Fully specified	Fully specified
CBTLV	CMOS	3.3 V	Fully specified	Fully specified	Not specified
LVxxxA	CMOS	3.3 V	Fully specified	Fully specified	Not specified
LVCxxxA	CMOS	3.3 V	Fully specified	Fully specified	Fully specified

The CMOS process indicates that both the input and the output structures comprise pure CMOS circuitry, whereas, the BiCMOS process indicates that both bipolar and CMOS transistors are implemented in the data or control input circuitry and/or output circuitry.

Power-Consumption Considerations

With the reduction of the supply voltage, a proportional power saving results. This section provides comparisons of the power consumption of logic families at different voltage levels.

The total power consumption of an integrated circuit is the sum of quiescent power dissipation, or static power consumption, (see Equation 1) and dynamic power consumption (see Equation 2). Dynamic power consumption consists of two parts:

- The average power dissipation caused by current spikes (see Equation 3). This is the power consumption that is caused by the internal circuitry of the logic device.
- The power dissipation caused by driving an externally connected load (see Equation 4).

Static power consumption: $$P_{STAT} = V_{CC} \times I_{CC} \quad (1)$$

Dynamic power consumption: $$P_{DYN} = P_T + P_L \quad (2)$$

Transient power consumption: $$P_T = V_{CC}^2 \times C_{PD} \times f_I \times N_{SW} \quad (3)$$

Capacitive-load power consumption: $$P_T = V_{CC}^2 \times C_L \times f_{OI} \times N_{SW} \quad (4)$$

Where:

V_{CC} = supply voltage
C_L = load capacitance
C_{PD} = dynamic power-dissipation capacitance
f_I = input-signal frequency
f_O = output-signal frequency
I_{CC} = supply current
N_{SW} = number of outputs switching

A reduction of V_{CC} directly results in a power savings. The relation in the static power consumption is linear (assuming that static I_{CC} is independent of V_{CC}), while the term V_{CC} is included as a squared factor within the dynamic power consumption formulas (see Equation 3 and Equation 4).

Using equations 1 through 4, a 3.3-V V_{CC} system theoretically saves between 33% for the static considerations (see Equation 1) and up to 57% for the dynamic case, when compared to 5-V systems. With a 2.5-V V_{CC}, the system's power consumption decreases to between 50% (static) and 75% (dynamic), respectively, compared to the 5-V system.

The data sheets of the logic families do not show all information about power consumption. One parameter that is shown for power consumption is the supply current (I_{CC}). However, in some cases, this parameter is given at only one supply voltage. The parameter I_{CC} is given in the table of electrical characteristics (recommended operation conditions) shown for the SN74LV245A in Table 2.

Table 2. LV245A Supply Current Parameter (I_{CC})

TEST CONDITIONS		V_{CC}	MIN	MAX	UNIT
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		20	μA

However, as previously mentioned, this parameter indicates the power consumption for static states only, either for the case that the input is statically set to V_{CC} or set to GND.

Another parameter that indicates the power consumption indirectly is the power-dissipation capacitance (C_{pd}) that is given, for example, for the AVC family at three supply voltages. With this parameter, the transient power consumption can be calculated using Equation 3.

For a more comprehensive overview of Texas Instruments logic families, measurements of the dynamic power consumption at different supply voltages have been taken. The logic families investigated were AHC, ALVT, ALVC, LVC, LV, and AVC.

The measurement setup is shown in Figure 2. For the measurement of dynamic power consumption, all but one input of the device under test (DUT) were set to a static high-state or low-state logic value. One input is connected to a signal generator. The applied signal is a square wave with a duty cycle of 50% and switches between the supply voltage of the DUT and GND. The frequency of the signal was varied between 1 MHz and 50 MHz and the supply current (I_{CC}) was measured within that range. The outputs of the DUT are not connected, so that only the device's internal power consumption, not the external load, is measured.

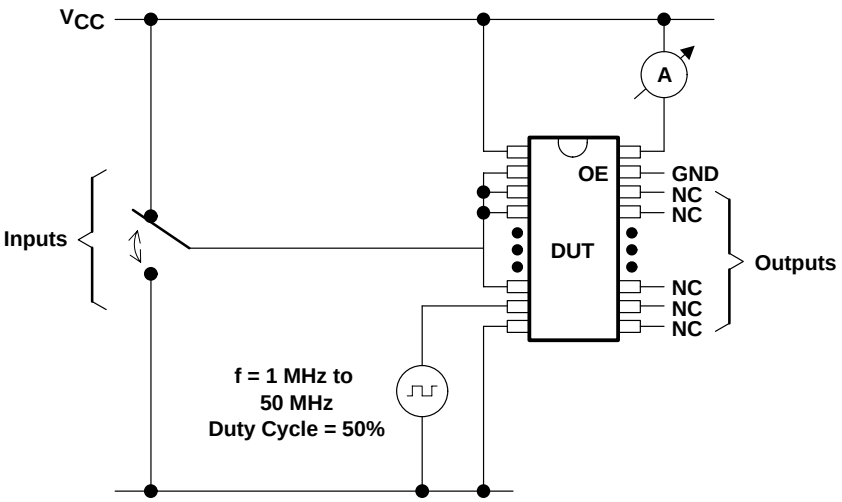


Figure 2. Power Consumption vs Frequency Measurement Setup

Figures 3 through 5 show the measurement results for 3.3-V, 2.5-V, and 1.8-V V_{CC}. The LVC and the AVC families have a specification for the 1.8-V V_{CC}, but the other logic families do not. However, the test samples of all investigated logic families showed full functionality at 1.8-V V_{CC}. For comparison, the power consumption has been measured at 1.8-V also.

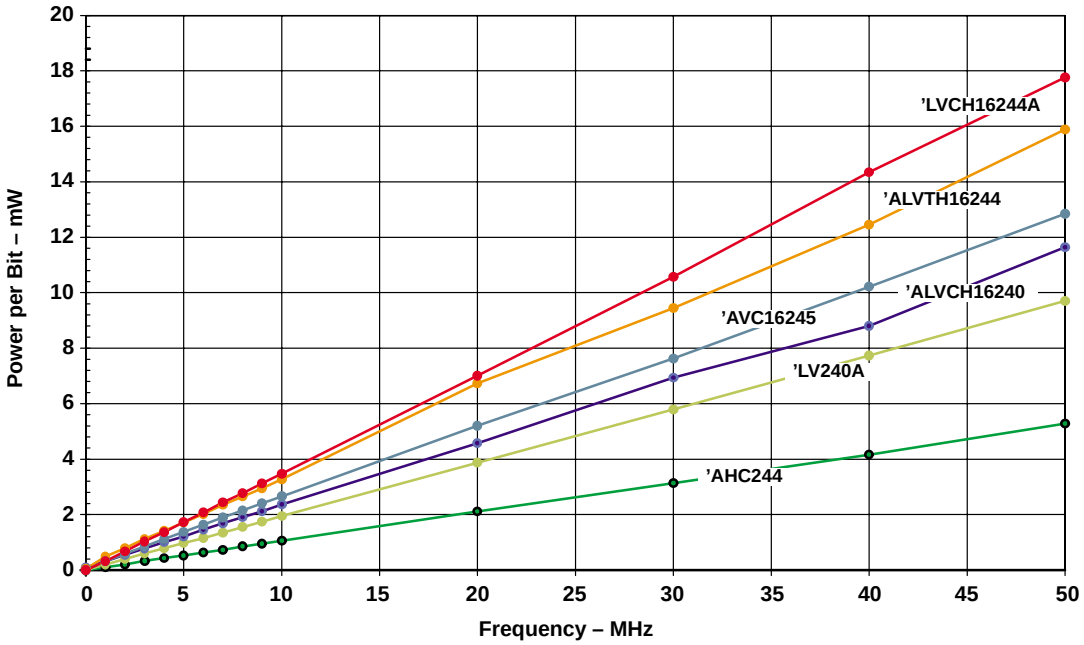


Figure 3. Power Consumption at 3.3-V V_{CC}

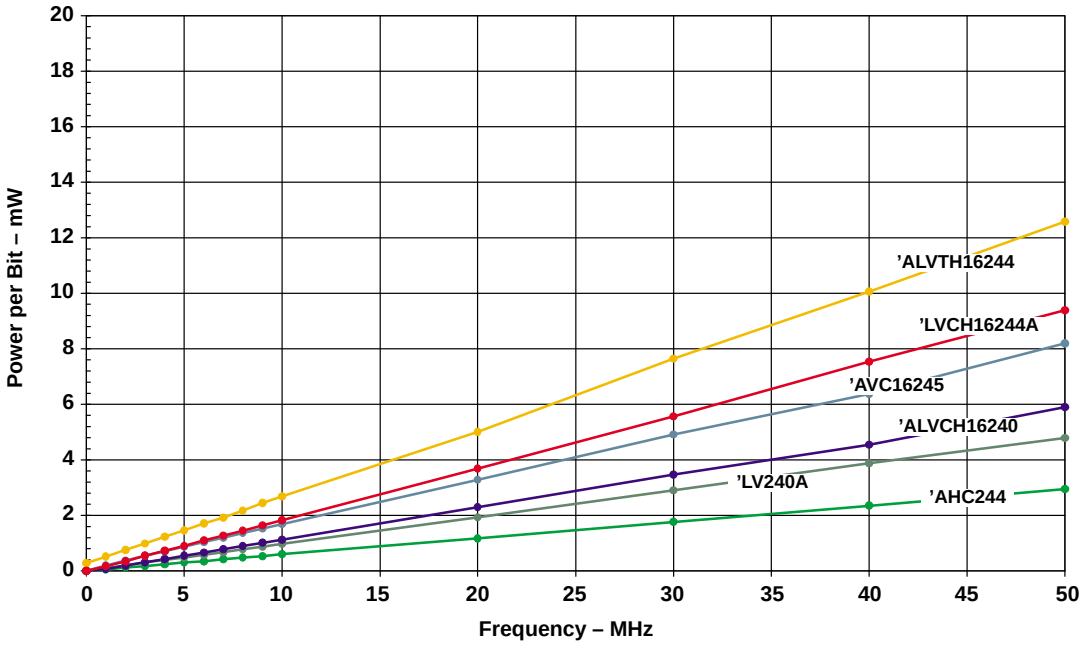


Figure 4. Power Consumption at 2.5-V V_{CC}

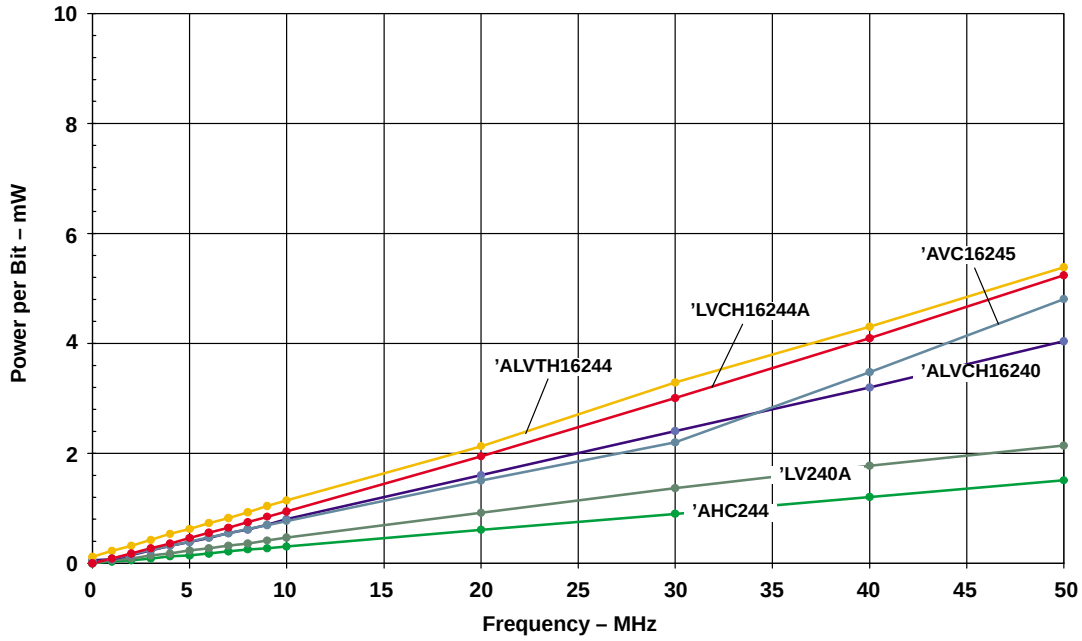


Figure 5. Power Consumption at 1.8-V V_{CC}

Figure 6 shows the relative power consumption of the tested logic devices compared to 3.3-V V_{CC}.

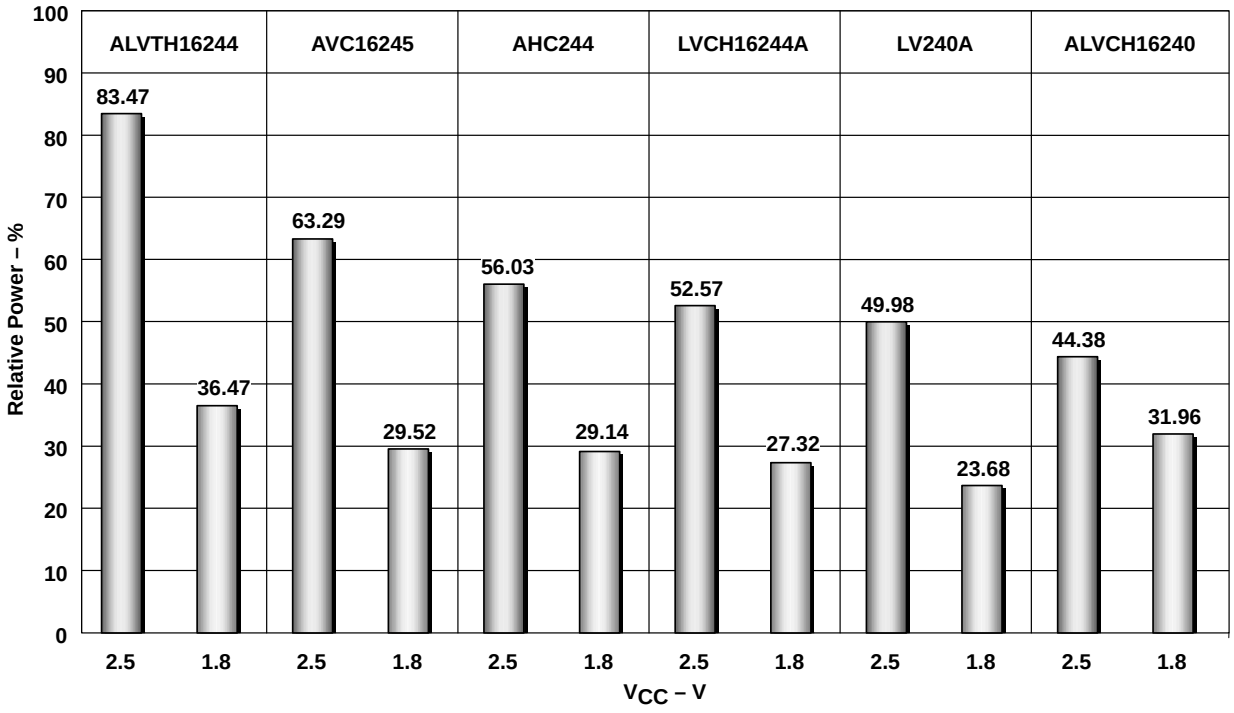


Figure 6. Relative Power Consumption at 2.5-V and 1.8-V V_{CC} Compared to 3.3-V V_{CC}

Output Characteristics at Less Than 3.3-V V_{CC}

Standard Logic Families

With the reduction of the supply voltage there is also a reduction of the drive capability of the logic circuit.

The output stage of a logic circuit in the high state behaves like a voltage source with an open-circuit voltage of V_{CC} for CMOS logic, and low-voltage BiCMOS logic, respectively.

In the low state, for positive voltages, the output resistance is based on the internal resistance of the conducting transistor, i.e., collector-emitter for BiCMOS technologies and drain-source resistance for CMOS technologies.

Negative voltage peaks at the inputs are limited by protection diodes. Output stages of the CMOS logic family SN74AHCxxx also have output protection diodes that connect output stages and V_{CC}. This diode limits the positive output voltage to V_{CC} + 0.5 V.

The available output current depends on V_{CC}, which determines the gate source voltage of the output transistors. At a supply voltage below about 1 V (less than the turn-on voltage of the MOS transistors) the output stays in the off state. With increasing supply voltage, output current increases also.

The LVC family has the dc characteristics shown in Table 3. The drive capability of this device decreases with decreasing supply voltage.

Table 3. LVCH245A Output Drive Parameters (V_{OH} and V_{OL})

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	I_{OH} = –100 μA	1.65 to 3.6 V	V_{CC} –0.2		V
	I_{OH} = –4 mA	1.65 V	1.2		
	I_{OH} = –8 mA	2.30 V	1.7		
	I_{OH} = –12 mA	2.70 V	2.2		
	I_{OH} = –12 mA	3.00 V	2.4		
	I_{OH} = –24 mA	3.00 V	2.2		
V_{OL}	I_{OL} = 100 μA	1.65 to 3.6 V		0.2	V
	I_{OL} = 4 mA	1.65 V		0.45	
	I_{OL} = 8 mA	2.30 V		0.7	
	I_{OL} = 12 mA	2.70 V		0.4	
	I_{OL} = 24 mA	3.00 V		0.55	

Figure 7 illustrates values of I_{OL} and I_{OH} and the corresponding values of V_{OL} and V_{OH} for a typical LVC device. The output characteristics of the LVC device were taken at 3.3-V, 2.5-V, and 1.8-V V_{CC}. The drive capability decreases significantly with reduced supply voltage. The same trend can be observed for all logic families.

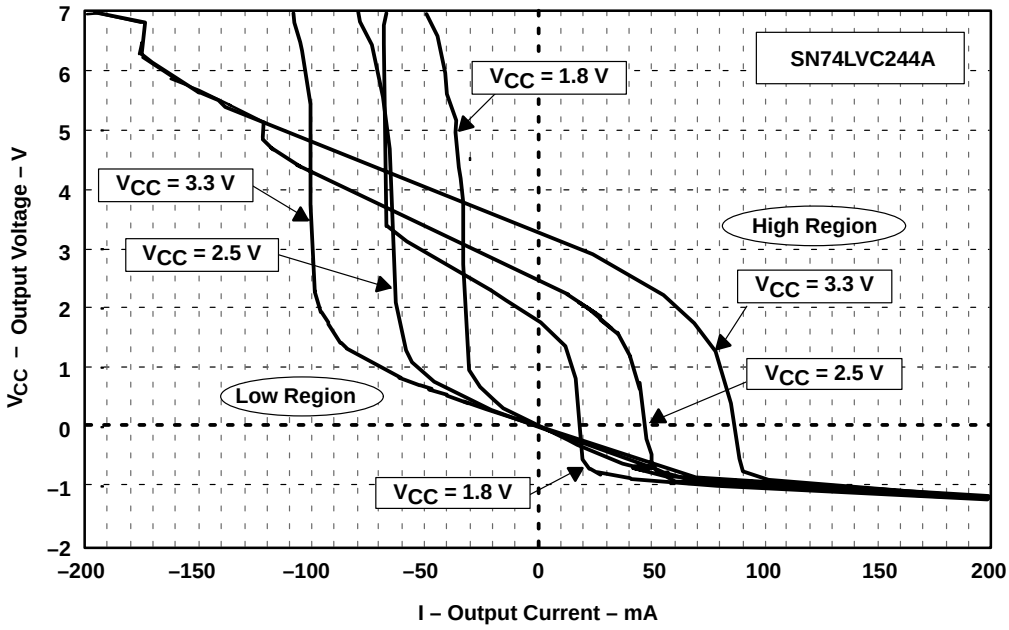


Figure 7. Output Characteristics of the LVC244 at Different Supply Voltages

Table 4 shows a comparison of the output-current specifications of the logic families discussed in this report. All families have full 3.3-V and 2.5-V specifications. LV and the AHC have additional 5.5-V drive specifications. The AVC and LVC families show full specifications regarding the high-level and low-level output voltage and output current in the data sheets at V_{CC} = 1.8 V.

Table 4. Output-Current Specifications as Shown in the Data Sheet

LOGIC FAMILY	V_{CC}	MINIMUM		MAXIMUM		SPECIFIED IN DATA SHEET
		V_{OH}	I_{OH}	V_{OL}	I_{OL}	
AHC	2 V	1.9 V	–50 μA	0.1 V	50 μA	No switching characteristic
	2.30 V					N/A
	3.00 V	2.48 V	–4 mA	0.44 V	4 mA	Yes
	4.5 V	3.8 V	–8 mA	0.44 V	8 mA	5-V specification
LV	2 V–5.5 V	V_{CC}–0.1 V	–50 μA	0.1 V	50 μA	Yes
	2.30 V	2 V	–2 mA	0.40 V	2 mA	Yes
	3.00 V	2.48 V	–8 mA	0.44 V	8 mA	Yes
	4.5 V	3.8 V	–16 mA	0.55 V	16 mA	5-V specification
LVC	1.65	1.2 V	–4 mA	0.45 V	4 mA	Yes
	2.30 V	1.7 V	–8 mA	0.70 V	8 mA	Yes
	2.70 V	2.2 V	–12 mA	0.40 V	12 mA	Yes
	3.00 V	2.2 V	–24 mA	0.55 V	24 mA	Yes
ALVC	1.65					Planned
	2.30 V	2 V	–6 mA	0.40 V	6 mA	Yes
	2.70 V	2.2 V	–12 mA	0.40 V	12 mA	Yes
	3.00 V	2 V	–24 mA	0.55 V	24 mA	Yes
ALVT	1.65					
	2.30 V	1.8 V	–8 mA	0.50 V	–24 mA	Yes
	3.00 V	2 V	–32 mA	0.55 V	–64 mA	Yes
AVC	1.65	1.2 V	–4mA	0.45 V	4 mA	Yes
	2.30 V	1.75 V	–8 mA	0.55 V	8 mA	Yes
	3.00 V	2.3 V	–12 mA	0.7 V	12 mA	Yes

Crossbar Technology (CBT)/Crossbar Technology Low Voltage (CBTLV)

The CBT families (SN74CBTxxx and SN74CBTLVxxx) are FET switches that do not have their own drive capability. They are a good solution in systems that require bus isolation and bus exchanging. The impedance of CBT devices varies with the amount of current flowing from the drain to the source. The data sheets reflect this with the parameter r_{on}.

Figure 8 shows the r_{on} measurement setup. Measurements were taken at 3.3-V, 2.5-V, and 1.8-V V_{CC} to show the influence of V_{CC} on r_{on} of the CBTLV3245A. The output was enabled by connection to GND.

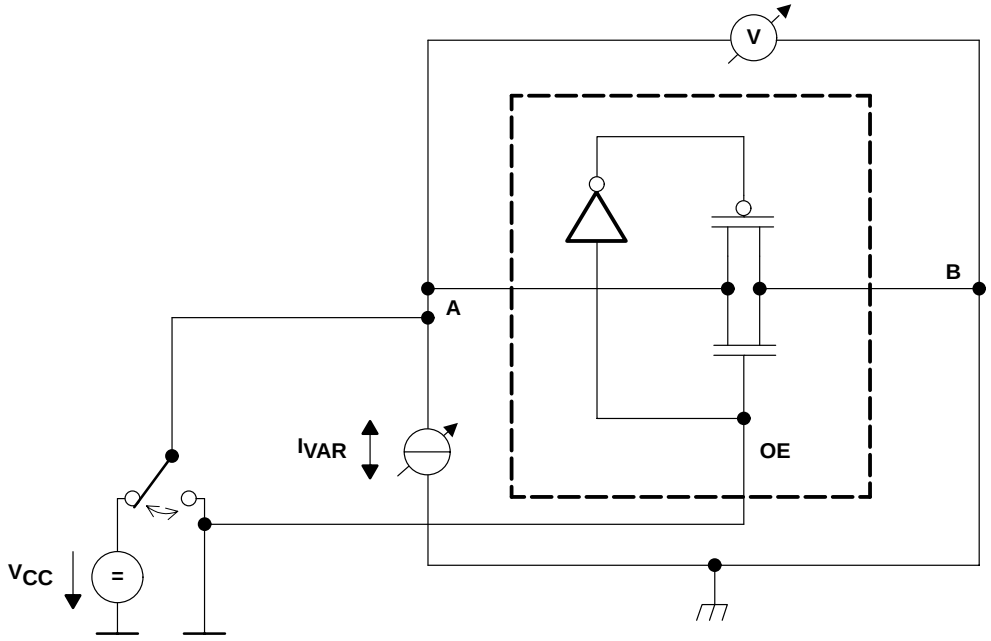


Figure 8. Setup for Measuring r_{on} of the CBTLV3245A

Input A was connected to V_{CC} to measure r_{on} in the high state. To measure r_{on} in the low state, input A was connected to GND of the supply voltage.

Also, input A was connected to a variable-current source that was swept from –200 mA to 200 mA. The voltage was measured over the drain-source of the CBTLV3245A between point A and point B.

Figures 9 and 10 show the measurement results. The linearity of r_{on} or the CBT3245A is best at 5.5-V V_{CC} with r_{on} (high state) of 10 Ω to 20 Ω and r_{on} (low state) of 4 Ω to 7 Ω.

The linearity of r_{on} for the CBTLV3245A is best at 3.3-V V_{CC} with r_{on} (high state) of 6 Ω to 10 Ω and r_{on} (low state) of 2 Ω to 5 Ω.

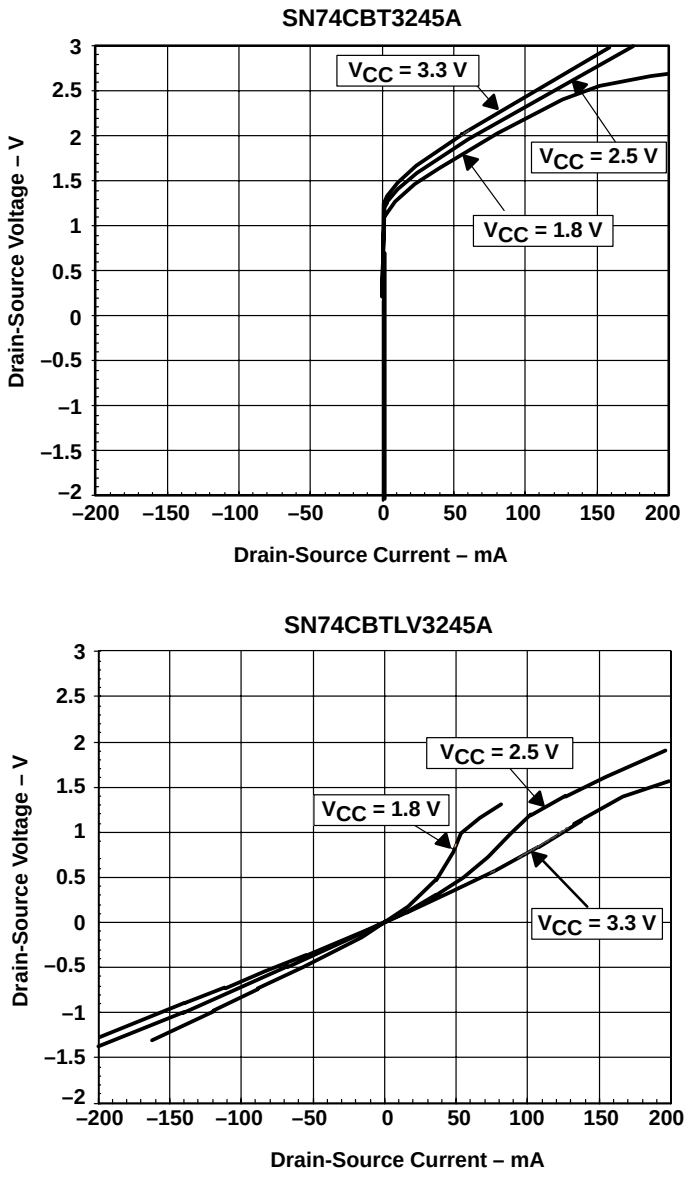


Figure 9. High-State r_{on} of CBT3245A and CBTLV3245A at Different Supply Voltages

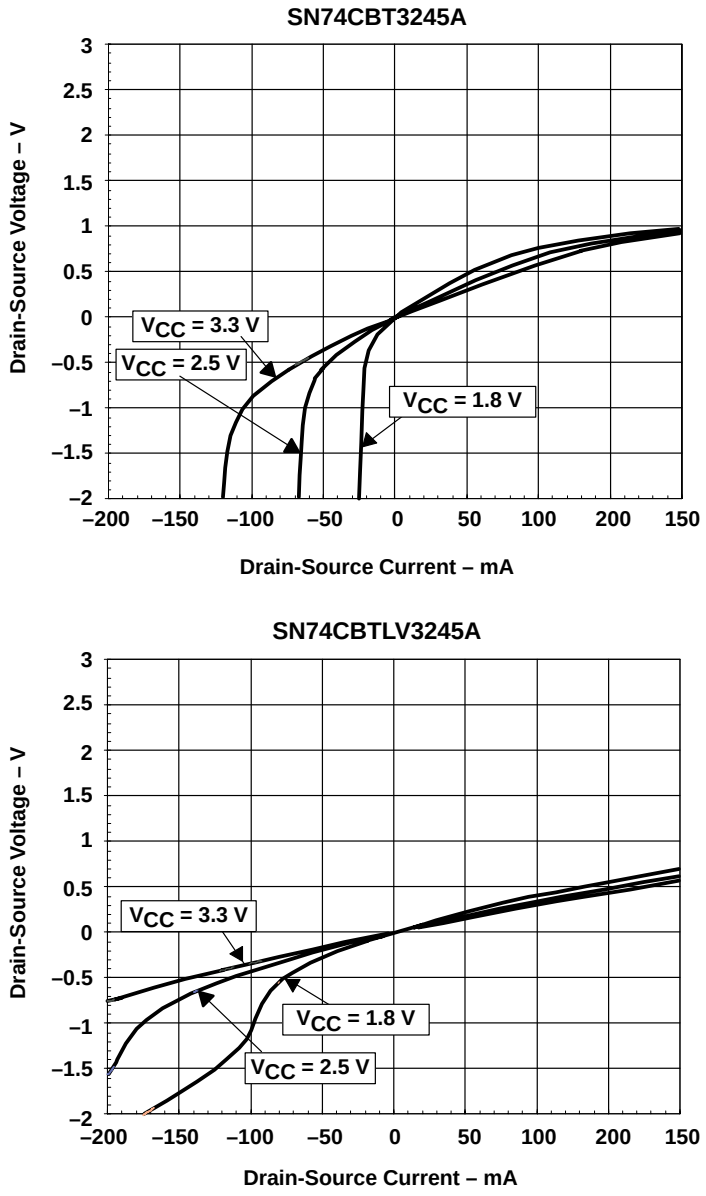


Figure 10. Low-State r_{on} of CBT3245A and CBTLV3245A at Different Supply Voltages

The linearity of r_{on} (drain-source) of the FET degrades with decreasing supply voltage. The CBT device conducts only if the drain-source voltage is more than approximately 1 V. The CBTLV devices are operational below this voltage because the P-channel FET is switched in parallel with the n-channel transistor and exhibits transmission-gate behavior. The r_{on} (high state) varies, depending on the conducted current and the supply voltage. The resistance values can be derived from Figures 9 and 10.

Propagation Delay Time at Different Supply Voltages

Decreasing a system's supply voltage from 5 V to 3.3 V, or lower, slows its speed (increases propagation time). This section contains a comprehensive collection of measurements that shows this effect. The data sheets show that the measurement setup for the propagation delay depends on the supply voltage of the device under test (DUT).

However, not only is the supply voltage reduced, but the measurement setup for the propagation delay time is different. Figure 11 shows the test condition for the measurements of the high-to-low and low-to-high propagation delay times at 5-V, 3.3-V, 2.5-V, and 1.8-V V_{CC}.

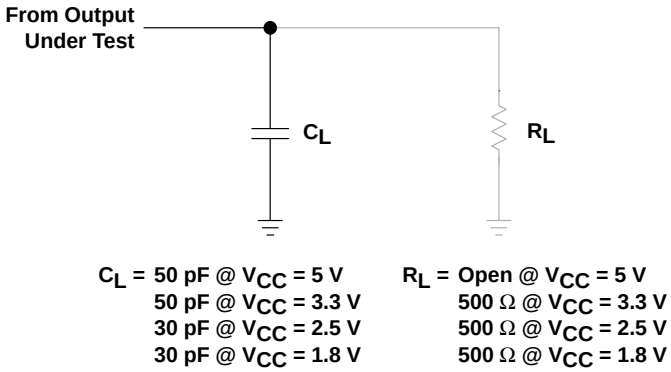


Figure 11. Test Conditions for Measuring Propagation Delay Time

While at 5-V V_{CC}, a 50-pF capacitor is the only load to the device's output, at 3.3-V V_{CC} a 500-Ω resistor (R_L) is in parallel with the capacitor for the measurement. At 2.5-V V_{CC} the value of the capacitor is reduced to 30 pF, and the value of the resistor in parallel is 500 Ω.

Figure 12 shows voltage waveforms. All input pulses are supplied by a generator having the following characteristics: signal frequency = 1 MHz, t_r, $t_f \leq 2.5$ ns. One output is measured at a time, with one transition per measurement.

For ALVTH at 3.3-V V_{CC}, the input signal was switched between 3.0 V and 0 V. In this case, the threshold voltage is 1.5 V. For all other measurements the input signal was switched between V_{CC} and GND and the threshold voltage chosen was $V_{CC}/2$.

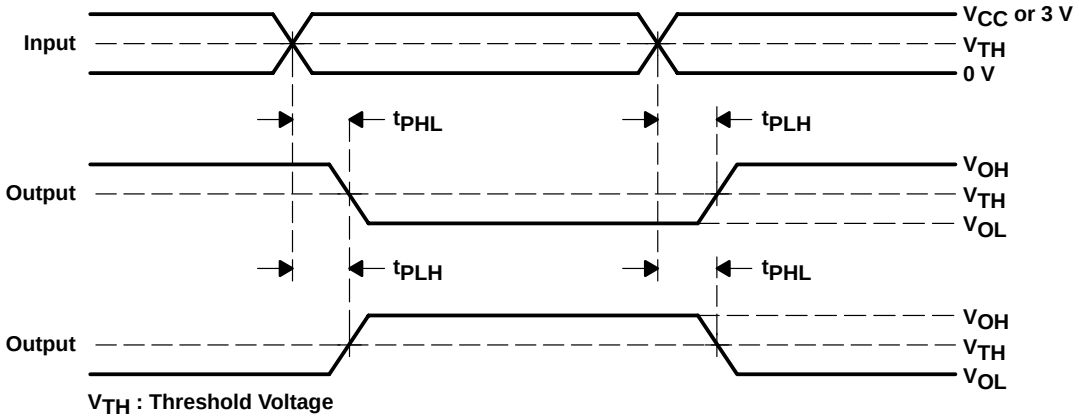


Figure 12. Propagation Delay Times of Inverting and Noninverting Outputs

Table 5 shows the results of the propagation delay time measurements. In Figure 13, the results are shown graphically for easier comparison.

Table 5. Typical Propagation Delays at Different Supply Voltages

SUPPLY VOLTAGE	LOAD CONDITION	t_{pd}	AHC244	LV240A	LVCH16244A	ALVCH16244	ALVTH16244	AVC16244	UNIT
5 V	C_L =50 pF	t_{PLH}	4.4	4.3	N/A	N/A	N/A	N/A	ns
		t_{PHL}	4.4	4.3	N/A	N/A	N/A	N/A	ns
3.3 V	C_L = 50 pF, R_L = 500 Ω	t_{PLH}	6.2	5.2	2.4	2.6	1.9	1.2†	ns
		t_{PHL}	5.5	4.9	2.0	1.7	1.5	1.6†	ns
2.5 V	C_L = 30 pF, R_L = 500 Ω	t_{PLH}	6.8	7.2	2.6	2.7	1.9	1.4	ns
		t_{PHL}	5.9	6.4	2.4	1.7	1.7	1.8	ns
1.8 V	C_L = 30 pF, R_L = 500 Ω	t_{PLH}	11.4	12.1	4.2	4.3	2.7	1.9	ns
		t_{PHL}	9.0	10.5	3.8	2.7	3.2	2.2	ns

† Measured with C_L= 30 pF

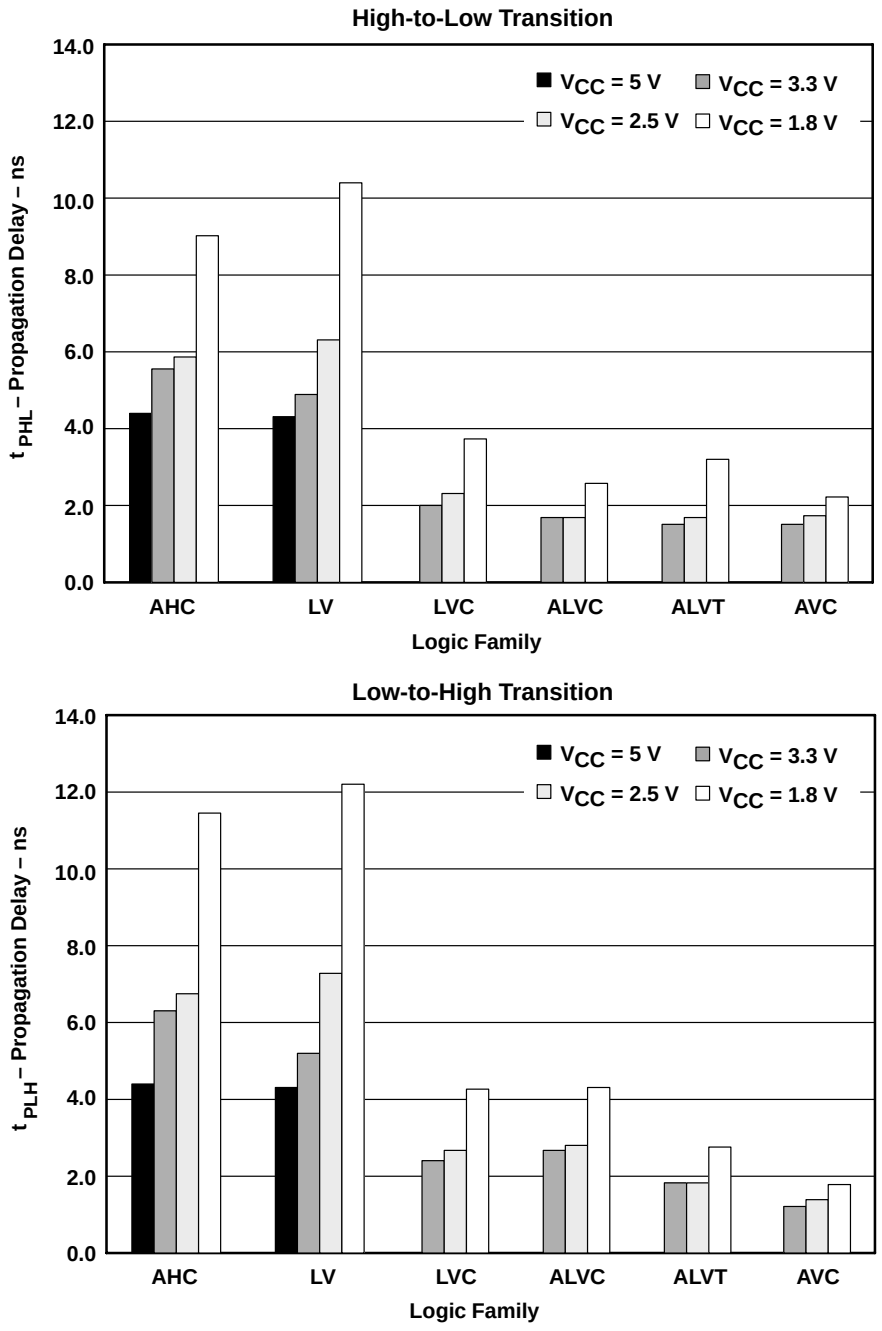


Figure 13. Typical Propagation Delays at Different Supply Voltages

With the AVC family, TI offers an optimized solution for the next low-voltage node of 2.5-V V_{CC}. This logic family is the fastest family in this comparison. Even when supplied with 1.8 V, the propagation delay time of the DUT is slightly less than 2 ns.

An application report, *AVC Logic Family Technology and Applications*, literature number SCES06, discussing the features and benefits of this 2.5-V logic, is available from TI.

Interfacing Between Different Voltage Levels

Regarding the term compatibility, possible interactions between logic devices that are supplied from different power-supply voltages must be considered. It is necessary to distinguish correctly between the terms tolerance, interfacing or translating, and level shifting. The input and output specifications are important for this discussion.

Input-Overvoltage Tolerance

A logic device is input-overvoltage tolerant if its input can withstand the presence of a higher voltage without being damaged. For example, the input-overvoltage tolerance is called 5-V tolerance if the device is powered from a 3.3-V, 2.5-V, or 1.8-V V_{CC} source and can accept a voltage level of 5 V at the inputs.

The input overvoltage tolerance is presented in the data sheet under the *recommended operating conditions* topic. The parameter is called V_I (input voltage). The LVC specification is shown as an example in Table 6.

Table 6. Extract of Recommended Operating Conditions for the LVCH245A

		MIN	MAX	UNIT
V_{CC}	Supply voltage	1.65	3.6	V
V_I	Input voltage	0	5.5	V

In this case, the input voltage (V_I) exceeds V_{CC}. This also implies that the device is tolerant of higher input voltage levels at every supply voltage between 1.65 V and 3.6 V. Table 7 shows the input overvoltage tolerance of the logic devices at the different supply voltages.

Table 7. Input-Overvoltage Tolerance of Different Logic Families

VOLTAGE (V_I) APPLIED TO INPUT	FAMILY AND SUPPLY VOLTAGE			
	ALVT, LVC, LVT, LV, AHC V_{CC} = 3 V TO 3.6 V	ALVT, LVC, LV, AHC V_{CC} = 2.3 V TO 2.7 V	LVC, LV, AHC V_{CC} = 2 V	LVC V_{CC} = 1.65 V
5 V	5-V tolerant	5-V tolerant	5-V tolerant	5-V tolerant
3.3 V		3.3-V tolerant	3.3-V tolerant	3.3-V tolerant
2.5 V			2.5-V tolerant	2.5-V tolerant

AVC logic has 3.3-V input-overvoltage tolerance with 2.5-V V_{CC} or 1.8-V V_{CC} and 2.5-V V_{CC} input-overvoltage tolerance with 1.8-V V_{CC}.

Output-Overvoltage Tolerance

A logic device is output-overvoltage tolerant if it can withstand the presence of a higher voltage during the high-impedance state at the output without being damaged.

The output-overvoltage tolerance is in the data sheet in the recommended operating conditions table as the parameter V_O. An example specification for the SN74LV245A is shown in Table 8.

Table 8. Extract of Recommended Operating Conditions for the LV245A

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	3.6	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	

During the logic high state, the device's output must not be connected to a higher voltage than V_{CC}; otherwise, the pullup transistor of the output stage will begin operation in reverse mode and a significant current could flow into the output of the device. This will prohibit a higher voltage logic level than V_{CC} and, under worst case conditions, damage the logic device.

Table 9 summarizes the output-overvoltage tolerance during the high-impedance state.

Table 9. Output-Overvoltage Tolerance of Different Logic Families

APPLIED VOLTAGE DURING THE HIGH-IMPEDANCE STATE	FAMILY AND SUPPLY VOLTAGE			
	ALVT, LVC, LVT, LV V_{CC} = 3 V TO 3.6 V	ALVT, LVC, LV V_{CC} = 2.3 V TO 2.7 V	LVC, LV V_{CC} = 2 V	LVC V_{CC} = 1.65 V TO 1.95 V
5 V	5-V tolerant	5-V tolerant	5-V tolerant	5-V tolerant
3.3 V		3.3-V tolerant	3.3-V tolerant	3.3-V tolerant
2.5 V			2.5-V tolerant	2.5-V tolerant

The LVT logic family is 5-V overvoltage tolerant (inputs and outputs) at 3.3-V V_{CC}. The ALVT, LVC, and LV families are 5-V overvoltage tolerant (inputs and outputs) at 3.3-V and 2.5-V V_{CC}. The LVC family also is 5-V overvoltage tolerant (inputs and outputs) at 1.8 V V_{CC}.

The AVC family is 3.3-V output-overvoltage tolerant at 2.5-V and lower V_{CC}.

The specification of the ALVC logic family shows the maximum value of V_{CC} for the input and the output voltages that can be applied to the device inputs and outputs.

The AHC family is tolerant of higher voltages only at the input. At the output, AHC devices have clamping diodes to V_{CC} such that an overvoltage applied to the output results in a current that flows through the clamping diode within the device to the internal V_{CC} connection.

Auto3-State Output of the ALVT Family

The auto3-state function that is implemented in the output of the ALVT family represents a specialty. The principle is shown in Figure 14.

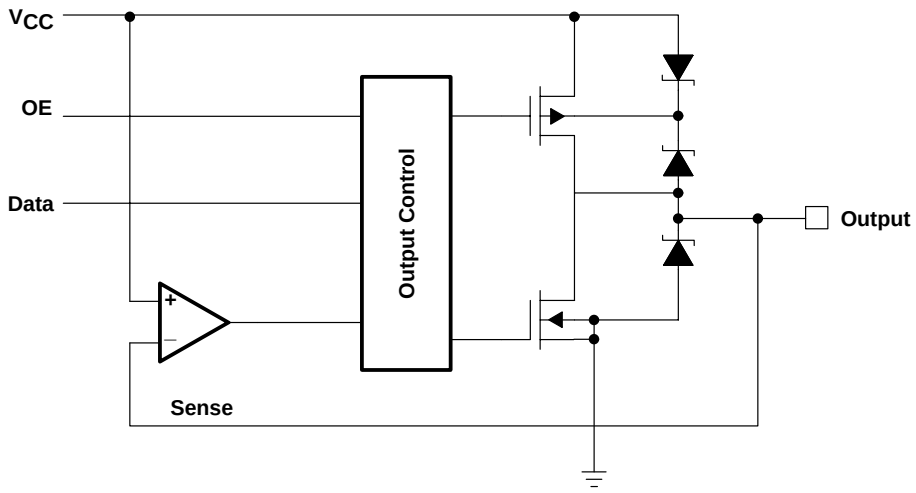


Figure 14. Simplified Auto3-state Output Stage of the ALVT Family

Assume that the output is in the active high state and a comparator monitors the voltage at the output and compares it with the supply voltage. If the voltage that is applied externally to the output exceeds the supply voltage, the output stage is switched to the high-impedance state. In this case, the logic levels that are applied to the data and control input pins of the device are irrelevant.

A current of about 30 mA is needed to reach V_{CC} + 0.6 V to trigger the auto3-state circuit, so that bus contentions are prevented, but switching noise will not trigger the auto3-state circuit. However, this also implies that the auto3-state cannot be achieved by the use of a simple pullup resistor.

It should be emphasized that a current can flow into the output only in the case of an active high. If the output is set to high impedance by the output enable (OE) control, no current will flow.

The series-opposed Schottky diodes always connect the back gate of the pullup transistor of the output stage to the higher voltage of V_{CC} or the voltage that is applied externally to the output. In this way, current flow from the output to V_{CC} is suppressed.

ALVTH logic has full overvoltage tolerance.

Translation Between Different Logic Levels

All of the logic families mentioned in this report can be operated and will function at 2.5-V and 3.3-V V_{CC}. The question is, how do they interact when one device is supplied with 2.5-V V_{CC} and the other with 3.3-V V_{CC}.

The overview of the different-level specifications from Figure 1 shows that the signal transfer from a 3.3 V V_{CC} (or higher supply voltage) logic to a 2.5-V V_{CC} logic will work perfectly if the 2.5-V part has overvoltage tolerance.

V_{OL} (3.3 V) = 0.4 V is lower than V_{IL} (2.5 V) = 0.7 V, having a noise margin of 300 mV, and V_{OH} (3.3 mV) = 2.4 V is greater than V_{IH} (2.5 V) = 1.7 V, resulting in a noise margin of 700 mV.

However, signal transfers in the opposite direction, from a 2.5-V logic to a 3.3-V (or higher supply voltage) logic is more critical. The low-level noise margin with V_{OL} (2.5 V) = 0.4 V and V_{IL} (3.3 V) = 0.7 V equals 300 mV. But the high-level definitions show that V_{OH} (2.5 V) = 2.0 V equals the input high limit of the 3.3-V V_{CC} logic V_{IH} (3.3 V) = 2.0 V (Figure 1, 5-V, 3.3-V, and 2.5 V V_{CC} switching-level comparison). In this case, the interface does not have any noise margin.

Therefore, 2.5-V V_{CC} devices should not be used to drive 3.3-V V_{CC} devices.

Table 10 gives an overview of the output-level compatibility of different logic families at 5-V, 3.3-V, 2.5-V, and 1.8-V V_{CC}.

Table 10. Output-Level Compatibility of Logic Families at Different Supply Voltages

LOGIC FAMILIES	SUPPLY VOLTAGE	CAN GENERATE 5-V LEVELS†	CAN GENERATE 3.3-V LEVELS†	CAN GENERATE 2.5-V LEVELS†	CAN GENERATE 1.8-V LEVELS†
AHC, LV	5 V	Yes	Yes‡	Yes‡	Yes‡
AHC, LV, LVC, ALVC, ALVT, AVC	3.3 V	TTL levels only	Yes	Yes§	Yes§
AHC, LV, LVC, ALVC, ALVT, AVC	2.5 V	TTL levels, but no noise margin for V_{OH}	No noise margin for V_{OH}	Yes	Yes¶
LVC, AVC	1.8 V	No#	No#	No#	Yes

† Output voltage levels exceed required input threshold voltage of the subsequent input stage at the given supply voltage.
‡ Receiver logic needs 5-V input tolerance.
§ Receiver logic needs 3.3-V input tolerance.
¶ Receiver logic needs 2.5-V input tolerance.
# V_{OH}, V_{OL} don't match, V_{OL}, V_{IL} don't match

Table 10 shows that there is a need for level-shifting devices for the interface between 5-V (CMOS) and 3.3-V V_{CC}, as well as for the translation between 2.5-V and 3.3-V V_{CC} devices.

A logic-high level at the output of the 3.3-V V_{CC} device cannot reach the required input high level of the successive 5-V CMOS input stage. Interfacing the output of the 2.5-V V_{CC} to the successive 3.3-V V_{CC} device is possible; however, in this case, there is no noise margin.

5-V to 3.3-V Level Shifters

Level shifters were developed for interfacing 5-V V_{CC} CMOS and 3.3-V V_{CC} logic. The SN74LVC4245A and SN74ALVC164245 establish a connection between 3.3-V V_{CC} and 5-V V_{CC} systems. These noninverting bus transceivers use two separate power-supply rails. The voltage ranges are defined as V_{CCA} = 4.5 V to 5.5 V and V_{CCB} = 2.7 to 3.6 V. The pin layout was designed such that they are directly replaceable by the standard devices SN74xxx245 and SN74xxx16245.

Furthermore, the SN74LVCC4245A is available for the 3.3-V to 5-V CMOS interfacing. The A-port V_{CCA} is dedicated to accepting a 5-V supply level, and the configurable B port, which is designed to track V_{CCB}, accepts voltages from 3 V to 5 V. This allows for translation from a 3.3-V V_{CC} to a 5-V V_{CC} environment, and vice versa. The LVCC4245A allows the voltage-source pin and I/O pin on the B port to float when V_{CCA} is supplied, such that there will be no disturbances on the A port if V_{CCB} and B-port I/O pins are not connected. The device will not operate until V_{CCA} and V_{CCB} are applied. This allows buffering data to and from PCMCIA sockets, permitting PCMCIA cards to be inserted and removed during operation.

Figure 15 shows the pinouts of the SN74ALVCH164245 and the SN74LVC4245A/'LVCC4245A.

2.5-V to 3.3-V/5-V SN74LVCC3245A Level Shifter

The SN74LVCC3245A level shifter gives more flexibility for level shifting. The A-port V_{CCA} is specified for the supply-voltage range of V_{CCA} = 2.3 V to 3.6 V and V_{CCB} = 3 V to 5.5 V. This allows for translation from a 2.5-V or 3.3-V environment to 3.3-V or 5-V logic levels, and vice versa. The SN74LVCC3245A is an appropriate solution for all interfacing applications from 2.5-V or 3.3-V logic levels to 3.3-V and/or 5-V CMOS.

The LVCC3245A, like the LVCC4245A, allows the V_{CCB} voltage-source pin and I/O pin on the B port to float when outputs are disabled. This allows buffering data to and from PCMCIA sockets that permit PCMCIA cards to be inserted and removed during operation.

The pinout of the SN74LVCC3245A is shown in Figure 15.

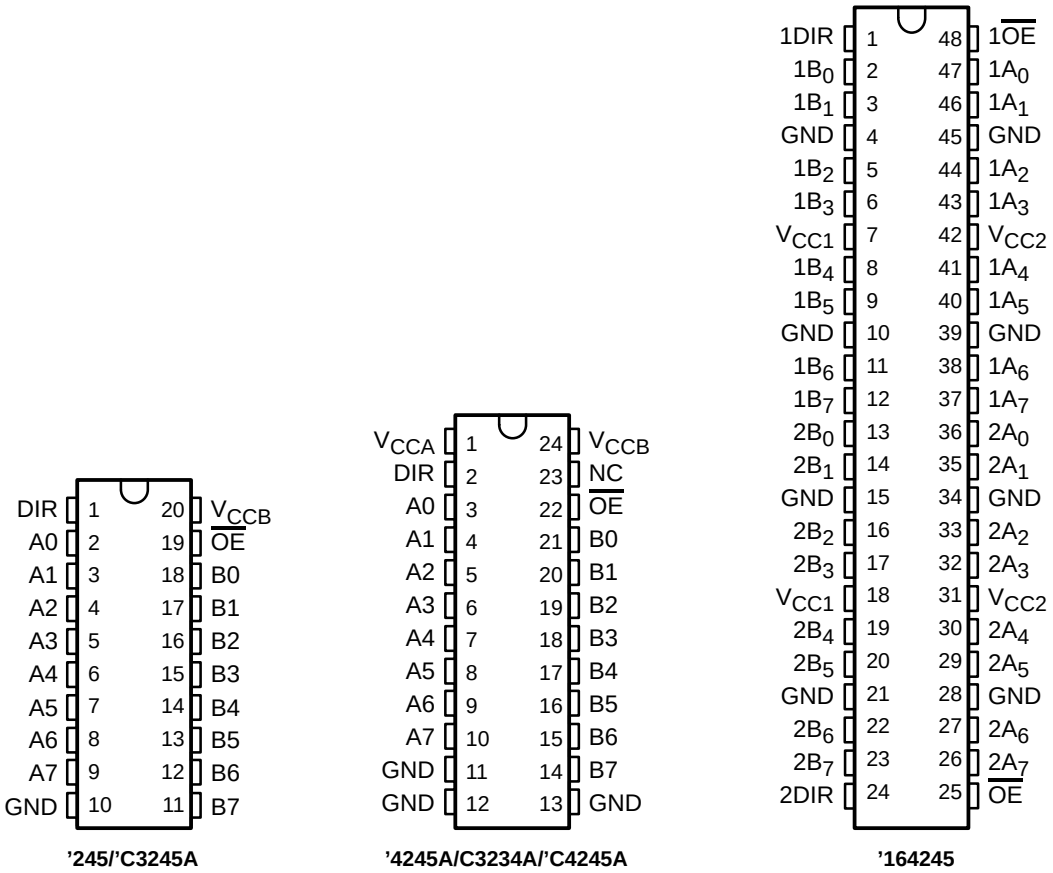


Figure 15. Pinouts of the LVCC3245A, LVCC4245A, LVC4245A, and ALVC164245

Open-Drain Drivers for Level Shifting

Another option for interfacing different logic levels is the use of open-drain devices. An open-drain output includes a pulldown transistor with the drain connect left open. An external connection via a pullup resistor is necessary. If the output transistor sinks current at the output, a logic-low state results. If the transistor is turned off, the logic-high state is forced by the pullup resistor, which is connected to V_{CC}.

Figure 16 shows the principle of an open-drain output interface. The value of R_{PULLUP} can be calculated from current requirements of inputs of the connected receivers, and R_{PULLUP} must be high enough to limit current into the conducting transistor.

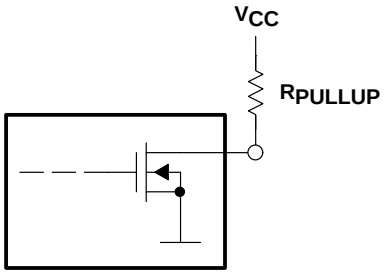


Figure 16. Open-Drain Output Principle

Table 11 shows the maximum voltage values that can be applied to the inputs and outputs of the available open-drain devices.

Table 11. Output-Overvoltage Tolerance at Open-Drain Drivers

	MAXIMUM VOLTAGE AT INPUT	MAXIMUM VOLTAGE AT OUTPUT
SN74AHC05	5.5 V	V_{CC}
SN74LV05	5.5 V	V_{CC}
SN74LVC06A	5.5 V	5.5 V
SN74LVC07A	5.5 V	5.5 V

Table 12 gives the level-shifting options for the SN74LVC07A between the different logic levels. The level shifting is possible because the pullup resistor effectively connects the output of the device to any required V_{CC}. Therefore, the correct switching level is provided to the input of the successive logic device. However, the maximum parameter values of the device, i.e., I/O voltages and current, must not be exceeded.

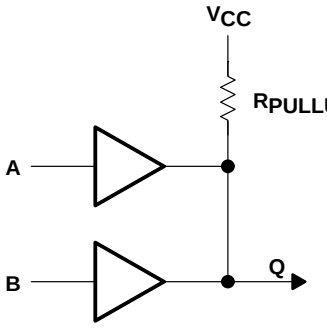
Table 12. Level Shifting Using the SN74LVC07A

SUPPLY VOLTAGE V_{CC1}	LVC07A UNDERSTANDS	PULLUP RESISTOR CAN BE CONNECTED TO	LEVEL CONVERSION RANGE
1.8 V	1.8-V levels	1.8 V, 2.5 V, 3.3 V, and 5 V	1.8 V to 1.8 V to 5.5 V
2.5 V	2.5-V levels	1.8 V, 2.5 V, 3.3 V, and 5 V	2.5 V to 1.8 V to 5.5 V
3.3 V	3.3-V levels	1.8 V, 2.5 V, 3.3 V, and 5 V	3.3 V to 1.8 V to 5.5 V
5 V	5-V levels	1.8 V, 2.5 V, 3.3 V, and 5 V	5 V to 1.8 V to 5.5 V

Wired Links

Another benefit from open-drain devices is that additional logic functionality can be built into a system without the need for additional gate devices. An active-low wired-OR and an active-high wired-AND can be implemented.

Figure 17 shows a wired connection and the resulting function table.



FUNCTION TABLE

A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

Figure 17. Wired Links Using Open-Drain Connections

The output (Q) is high when all inputs are high, resulting in an AND function in the case of a high-active-logic definition, and resulting in an OR function in the case of a low-active-logic definition. Those phantom links on the output side can be used to reduce component count. This kind of application is useful because a gate with n inputs can be implemented without extra active components.

Summary

The trend toward lower supply voltages continues unabated because the complexity of integrated circuits such as ASIC, CPU, and DSP requires continual reduction in structure size.

With the LV, LVC, ALVC, ALVT, AVC, and CBTLV logic families, TI offers options that are solutions for 2.5-V V_{CC} systems.

The measurement data shows that the propagation delay time of today's 3.3-V logic families varies at V_{CC} = 2.5 V from below the 2-ns range (AVC, ALVT) to 7 ns (LV). The drive capability (I_{OH}/I_{OL}) of the devices, which were investigated at 2.5-V, varies between ±2 mA (LV) and –8 mA/24 mA (ALVT). Consequently, a suitable logic family for most of the 2.5-V applications already is available.

At 1.8-V V_{CC} the devices show good performance as well, although the SN74LVCxxxA and SN74AVC logic families are fully specified at this V_{CC} only.

All investigated samples are fully operational at 1.8 V. The migration from 3.3-V V_{CC} to 1.8-V V_{CC} can result in power savings up to 76 percent.

The logic families ALVT, LVC, and LV show full overvoltage I/O tolerance at 1.8-V, 2.5-V and 3.3-V V_{CC}.

Options on bidirectional interfacing of different logic levels are given, with the level shifters that enable bidirectional level shifting from 2.5 V to 5.5 V.

Another option enabling even more flexibility is the open-drain driver, SN74LVC07A, that interfaces 1.8-V up to 5.5-V logic levels.

Acknowledgment

The author of this report is Johannes Huchzermeier.

Glossary

A

ABT	Advanced BiCMOS Technology
AC	Advanced CMOS
AHC	Advanced High-Speed CMOS
ALS	Advanced Low-Power Schottky
ALVC	Advanced Low-Voltage CMOS
ALVT	Advanced Low-Voltage Technology
AS	Advanced Schottky
Auto3-state	During the active-high state at the output, devices with auto3-state tolerate a higher voltage level at the outputs. This is also called overvoltage protection.
AVC	Advanced Very Low-Voltage CMOS

B

BCT	BiCMOS Technology
BiCMOS	Combination of Bipolar and CMOS processes: CMOS input structure and bipolar output structure
Bus hold	Input circuitry that holds the last valid logic state that was applied to it before entering a nondefined state on the bus until a new valid logic state is driven actively.

D

DUT	Device under test

G

GND	Ground

I

I_{CC}	Supply current
I/O	Input/Output

L

LS	Low-Power Schottky
LV	Low-Voltage CMOS, originally designed for V_{CC} = 3.3-V, also specified at 5 V
LVC	Low-Voltage CMOS
LVT	Low-Voltage Technology

O

Overvoltage protection	See auto3-state and 3-/5-V tolerance

R

R_L	Load resistor
R_{PULLUP}	Resistor that is used for open-drain devices to ensure a logic-high level on the signal line
ROC	Recommended operating conditions

S

Series resistor	A resistor that is implemented on the output stage of a bus driver. With this resistor, the effective output impedance of the driver is shifted to a value of about 50 Ω, which is an optimum line termination.
S	Schottky
SPICE	Simulation Program with Integrated Circuit Emphasis

T

3-/5-V tolerance	Logic devices with 5-V (3.3-V) tolerance tolerate 5-V (3.3-V) CMOS logic levels at their input and output during the high-impedance state, while supplied with 2.5-V
TTL-level	Transistor-transistor logic levels

V

V_{CC}	Supply voltage

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